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Large-Area Fabrication of Patterned ZnO-Nanowire Arrays Using Light Stamping Lithography

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ABSTRACT We demonstrate selective adsorption and alignment of ZnO nanowires on patterned poly(dimethylsiloxane) (PDMS) thin layers with (aminopropyl)siloxane self-assembled monolayers (SAMs). Light stamping lithography (LSL) was used to prepare patterned PDMS thin layers as neutral passivation regions on Si substrates. (3-Aminopropyl)triethoxysilane-based SAMs were selectively formed only on regions exposing the silanol groups of the Si substrates. The patterned positively charged amino groups define and direct the selective adsorption of ZnO nanowires with negative surface charges in the protic solvent. This procedure can be adopted in automated printing machines that generate patterned ZnO-nanowire arrays on large-area substrates. To demonstrate its usefulness, the LSL method was applied to prepare ZnO-nanowire transistor arrays on 4-in. Si wafers.

KEYWORDS: light stamping lithography • ZnO nanowire • patterning • self-assembly • field-effect transistor

1. INTRODUCTION

Controlling the alignment and positioning of nanowires is essential to the construction of various nanowire devices, such as field-effect transistors (FETs) (1−4), crossed junctions (5), rotational actuators (6), chemical and biological sensors (7−9), and flexible electronic devices (9). There are several fabrication methods for the assembly and alignment of nanowires and nanotubes, which include catalyst pattern-directed deposition (10), flow cell methods (11), capillary-force-driven assembly (12), electromagnetic-field alignment (13), and surface-pattern-directed assembly (14, 15). Among these methods, there has been a growing interest in forming patterned nanowire arrays by surface-pattern-directed assembly as a simple low-cost fabrication process, where the attractive interactions between surface patterns and nanowires in the solution direct the alignment of nanowires without any external forces (14−17).

Soft lithography is the most efficient method to fabricate surface patterns on planar, curved, or flexible substrates at low cost (18, 19). Soft lithography includes a number of nonphotolithographic techniques that use a patterned elastomer [primarily poly(dimethylsiloxane) (PDMS)] as a stamp, mold, or mask to transfer the pattern to substrates. Among these techniques, microcontact printing is the most versatile and cost-effective method that can routinely form patterned self-assembled monolayers (SAMs), i.e., thin organic films that form spontaneously on solid surfaces (20−22). They can be used as templates for selective adsorption and alignment of nanowires in surface-pattern-directed assembly (12−17). Microcontact printing is a low-cost technique that can generate patterns on nonplanar surfaces. Even though microcontact printing shows great promise in micro/nanofabrication, critical issues remain to be solved, for example, poor edge resolution, low thermal stability and density of defects of the patterned SAMs, and, especially, difficulty with automated and multiple printing (19−22).

Recently, we developed a new soft-lithographic method for generating a patterned PDMS film on a variety of solid substrates, i.e., light stamping lithography (LSL) (23). In the LSL method, the features of a patterned PDMS stamp are physically torn and transferred onto a substrate via a UV (254 nm)-induced surface reaction that results in bonding between the PDMS stamp and the substrate. LSL consists of three key steps, as described in detail previously. First, a patterned PDMS stamp is fabricated and brought into contact with a substrate surface. Second, the substrate is exposed through the PDMS stamp to a 254-nm UV lamp for 2 min, which induces the formation of chemical bonds between the PDMS stamp and the substrate. Finally, the PDMS stamp is physically peeled off from the substrate, with torn pieces remaining thereon.

Owing to the simple activation and bonding process, the LSL method appears to have several potential advantages over other soft-lithographic methods. Alignment of the PDMS stamp can be easily inspected, and errors can be corrected immediately. In the LSL method, the position of the stamp can be adjusted even after its contact with the substrate because the pattern is not transferred to the substrate without UV irradiation. Compared to microcontact printing, the PDMS stamp in this method can be used repeatedly without any treatment. The elastomeric proper-

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Received for review August 27, 2009 and accepted October 9, 2009

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DOI: 10.1021/am900580v

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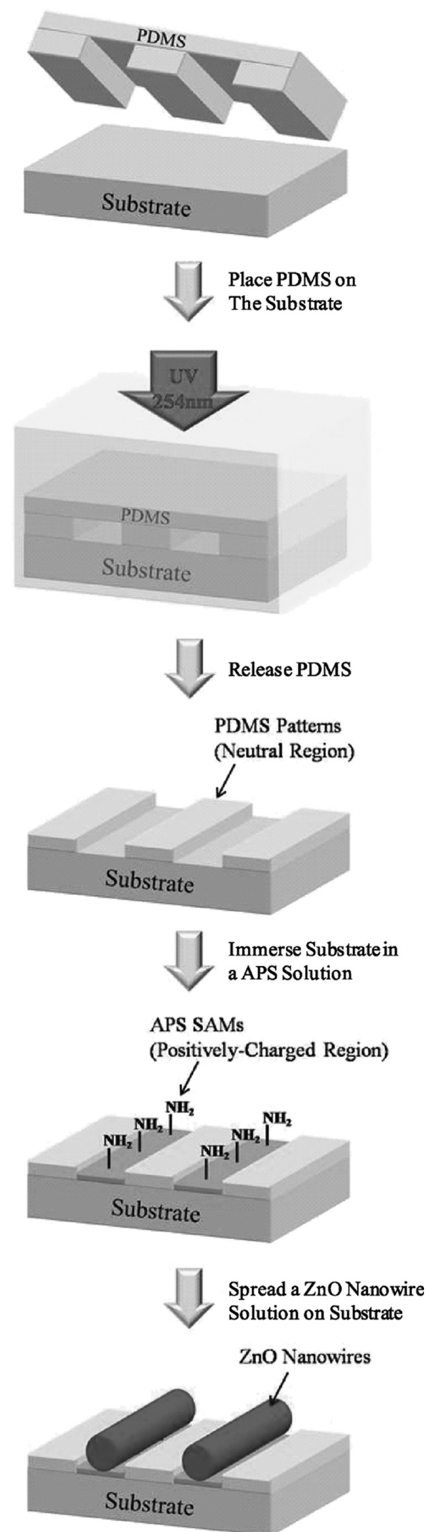
ties of the PDMS stamp allow it to recover its original shape, even after undergoing many cycles of pattern transfer. Because treatment of the stamp is not required, continuous printing is possible on diverse substrates as long as PDMS can be bonded to the substrate by the irradiation of UV light. We believe that the LSL method can be adopted in automated printing machines that are used to generate patterns with a wide range of feature sizes on diverse substrates. The PDMS patterns thus prepared can be used as templates for the selective adsorption and alignment of nanowires.

Here we report a new fabrication method of patterned ZnO-nanowire arrays using LSL. ZnO nanowires have attracted particular attention because of their potential for application in functional devices, such as FETs (24), optical devices (25, 26), chemical sensors (27), and electrochemical actuators (28, 29). Our approach consists of three key steps, as shown in Scheme 1. First, patterned PDMS thin layers were formed on substrates using LSL. The patterned PDMS acts as a neutral passivation region on the substrate. Second, the remaining regions of the substrates were coated with (3-aminopropyl)triethoxysilane (APS)-based SAMs. Third, the ZnO nanowires in the solution were selectively adsorbed and aligned onto the SAM-patterned substrates. In this case, the positively charged NH_3^+ groups in the APS SAM patterns have attractive electrostatic interactions with the ZnO nanowires, which carry surface negative charges in the protic solvent, whereas the neutral CH_3 groups in the PDMS patterns have no interactions. This procedure defines and directs the selective adsorption and alignment of the ZnO nanowires generating patterned nanowire arrays on substrates.

Scheme 1. Schematic Outline of the Procedure To Fabricate Patterned ZnO-Nanowire Arrays by Surface-Pattern-Directed Assembly Using LSL



2. EXPERIMENTAL DETAILS

2.1. Materials. Octadecyltrichlorosilane [$CH_3(CH_2)_{17}SiCl_3$; Aldrich; 97%], (3-aminopropyl)triethoxysilane [$NH_2(CH_2)_3Si(OCH_2CH_3)_3$; Aldrich; 97%], hexane (Aldrich; anhydrous, 99%), hexadecane (Aldrich; anhydrous, 99%), chloroform (Aldrich; anhydrous, 99%), carbon tetrachloride (Aldrich; anhydrous, 99.5%), methanol (Aldrich; ACS reagent, 99%), ethanol (Aldrich; ACS reagent, 99%), and diethyl zinc [Et_2Zn; Aldrich; 96%] were used as received. Poly(dimethylsiloxane) (Sylgard 184) was ordered from Dow Corning. Deionized water was purified with a Millipore Milli-Q plus system, distilled over $KMnO_4$, and then passed through the Millipore Simplicity system.

2.2. Preparation of ZnO Nanowires. ZnO nanowires were grown on GaAs (002) substrates using metal–organic chemical vapor deposition with Et_2Zn and O_2 as precursors. Single-crystalline ZnO nanowires with about 0.5-μm diameter and 10-μm length were fabricated using a previously reported method (30, 31). The grown ZnO nanowires were removed from the GaAs substrates by a brief sonication in ethanol (30–60 s).

2.3. Preparation of Substrates. The Si substrates used in this research were cut from n-type (100) wafers with resistivity in the range 1–5 Ω cm. The Si substrates were initially treated by a chemical cleaning process proposed by Ishizaka and Shiraki, which involves degreasing, HNO_3 boiling, NH_4OH boiling (alkali treatment), HCl boiling (acid treatment), rinsing in deionized water, and blow-drying with nitrogen to remove contaminants (32). A thin protective oxide layer was grown on the Si substrate by chemical oxidation with peroxysulfuric acid. CH_3-terminated SAMs were formed by immersing the Si substrates in a 2.5 mmol solution of octadecyltrichlorosilane (OTS) precursor dissolved in hexadecane–chloroform (4:1). The samples were then washed in carbon tetrachloride to remove excess reactants and dried with nitrogen. The quality of the monolayers was checked by X-ray photoelectron spectroscopy (XPS) and water contact-angle measurements. The water contact angle was about 110°, and the $^{1s}C/^{2p}Si$ peak area ratio measured by XPS was about 1.7. NH_3^+-terminated SAMs were formed by immersing the Si substrates in a 10 mmol solution of the APS precursor dissolved in methanol–water (10:1) with

acetic acid. The samples were then washed in methanol to remove excess reactants and dried with nitrogen. The quality of the monolayers was checked by XPS and the water contact angle. The water contact angle was about 41°, and the ${}^{1s}N/{}^{2p}Si$ peak area ratio measured by XPS was about 0.12. The Si substrates modified with PDMS were fabricated by casting liquid PDMS on the substrates.

2.4. Formation of Molecular Patterned Substrates Using LSL. Several PDMS patterns were made on the oxidized Si substrates using the LSL method. The masters we used for the fabrication of stamps are silicon wafers with line-patterned resists, on scales from 3.5 to 200 μm. The stamps were fabricated by casting liquid PDMS on the masters. After curing, the PDMS stamps were peeled away from the masters. When the stamps were made using these masters, the raised lines of the master corresponded to the recessed spaces of the stamps. The patterned PDMS stamps were placed in contact with the oxidized Si substrates. Then, the substrates were exposed through the PDMS stamps to an ORIEL 450 W xenon lamp (UV-enhanced) with a total intensity of 50 mW/cm^2 at a working distance of 20 cm for 2 min. UV irradiation induces strong surface bonding between the PDMS stamps and the substrates because the primary wavelength of the lamp is 254 nm and PDMS is optically transparent above 230 nm. After surface reaction was induced, the stamps were peeled away carefully. The PDMS patterns were left on the substrates exclusively in the areas of contact. When the PDMS patterns were made using these stamps, the patterned hydrophobic, neutral regions were produced on the substrates.

2.5. Analysis Techniques. Atomic force microscopy (AFM) images of the samples were obtained on a PSIA XE-100 instrument operating in tapping mode. XPS measurements were conducted using ESCALAB MKII. Water contact angles of the samples were determined on a model A-100 Rame-Hart NRL goniometer in ambient air by using the sessile drop method. Scanning electron microscopy (SEM) images were obtained, using a Hitachi S4800. All current−voltage ($I-V$) properties of the ZnO-nanowire thin film transistors were measured with a semiconductor parameter analyzer (HP 4155C, Agilent Technologies) in ambient air (relative humidity ∼45%) at 20 °C in the dark.

3. RESULTS AND DISCUSSION

3.1. Surface Interactions between ZnO Nanowires and Various Substrates. The interactions between ZnO nanowires and planar substrate surfaces were examined as a function of their surface functionality. This study includes the use of clean oxidized Si(100) surfaces, surfaces modified with OTS and APS SAMs, and PDMS. The terminal groups of oxidized Si, OTS, APS, and PDMS surfaces are hydroxyl (OH), methyl (CH_3), amine (NH_2), and methyl (CH_3), respectively. A solution of suspended ZnO nanowires was spread on four different substrate surfaces. The substrates were rinsed by agitation in a clean bath, in order to remove nanowires bound by nonspecific interactions, presumably through dispersion forces between the nanowires and the substrate surfaces. Figure 1 shows the highly selective adsorption of the ZnO nanowires onto only NH_3^+-terminated surfaces. It is well-known that the surfaces of the ZnO nanowires and the clean oxidized Si are hydrophilic and negatively charged in protic solvents, whereas the Si surfaces modified with APS SAMs are hydrophilic and positively charged (15, 37). The CH_3-terminated Si surfaces coated by OTS SAMs and PDMS are hydrophobic and neutral in protic solvent (15, 23). Figure 1d shows that electrostatic attractive interactions between ZnO and NH_3^+-terminated surfaces immobilized the ZnO nanowires on the Si substrates coated by APS SAMs. Electrostatic repulsive forces and the lack of specific interactions between ZnO and the other surfaces resulted in mobile ZnO nanowires on the surface, which were rinsed by agitation in a clean bath, as shown in Figure 1a−c.

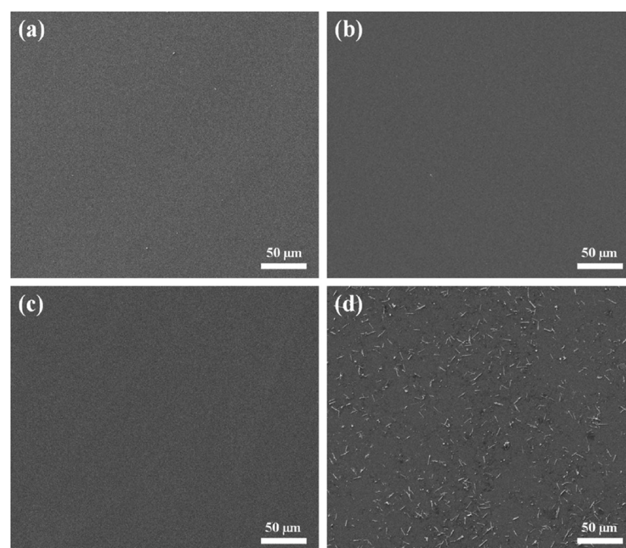


FIGURE 1. SEM images of ZnO nanowires on (a) clean oxidized Si(100), (b) OTS SAMs, (c) PDMS, and (d) APS SAMs.

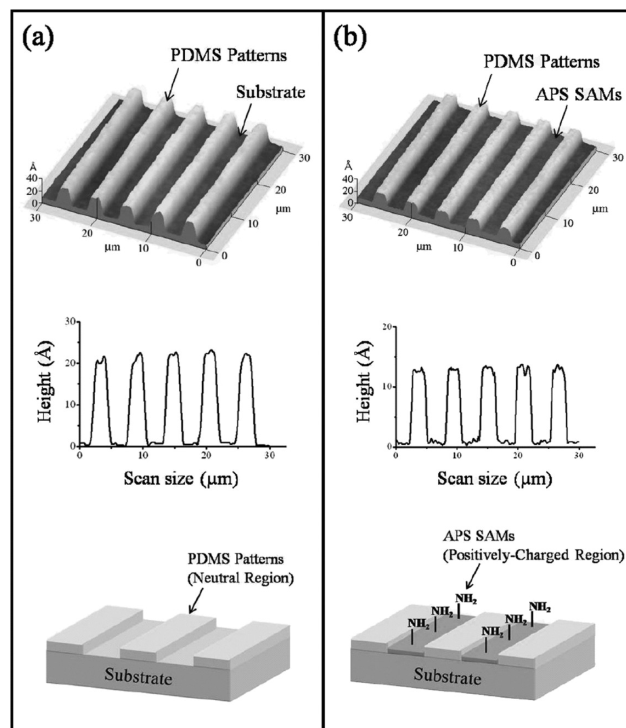


FIGURE 2. AFM images and cross sections: (a) PDMS patterns fabricated using LSL on Si substrates; (b) PDMS patterns after backfilling of the remaining regions with the APS SAMs.

3.2. Formation of Molecular Patterned Substrates Using LSL. Figure 2a shows a typical AFM image and a cross section of the PDMS patterns fabricated using the master having 3.5-μm parallel lines with 2.5-μm spaces.

This image clearly shows that the PDMS patterns retain the dimensions of the masters without noticeable line spreading. Additionally, the height of each PDMS pattern is about 21 Å, which is close to that of a densely packed alkylsiloxane monolayer (∼20 Å) (38−40). The water contact angle of the PDMS-patterned Si substrates was about 106°, which is close to that of the CH_3-terminated alkylsiloxane SAMs patterned on Si by microcontact printing (41−43). The PDMS-patterned Si substrates were then immersed in an APS solution for 5 min to coat the remaining regions of the substrates with NH_2-terminated alkylsiloxane SAMs. The height of the PDMS patterns is uniformly reduced by 8 Å after backfilling of the remaining regions with the APS SAMs, as shown in Figure 2b. This observation indicated that the remaining regions in the PDMS-patterned substrates were covered by high-quality APS SAMs because the height of a densely packed APS monolayer is about 8 Å (44). The regions covered by the PDMS pattern were hydrophobic, neutral surfaces, whereas the regions of exposed NH_2 groups were hydrophilic, positively charged surfaces.

3.3. Formation of Patterned ZnO Nanowires. A solution of suspended ZnO nanowires (about 0.5-μm diameter and 10-μm length) was spread on the patterned substrate surface. The nanowires were attracted to the positively charged NH_3^+ regions and aligned along the molecular patterns. When the patterned substrates were rinsed by agitation in a clean bath, the nanowires bound through nonspecific dispersion forces were removed from the neural PDMS regions, while the nanowires bound to the positively charged APS regions remained. Parts a−d of Figure 3 illustrate optical microscopy images of patterned ZnO nanowires, which were selectively adsorbed onto the monolayer-patterned Si substrate fabricated using a master having 30-, 70-, 90-, and 200-μm parallel lines with 30-, 30-, 20-, and 30-μm spacing, respectively. The ZnO nanowires are selectively immobilized only on the regions modified with APS SAMs. These images clearly show that the patterns of the ZnO naowires were defined and directed by the patterned SAMs generated with LSL.

Parts e and f of Figure 3 show SEM images of patterned ZnO nanowires, which were selectively adsorbed onto the prepatterned substrate with PDMS and APS SAMs. When the width of the APS SAM patterns is larger than the average length of the ZnO nanowires, the immobilized nanowires in the APS regions are randomly oriented, as shown in Figure 3e. However, the nanowires seem to align along the long axis of the line pattern with a small width of about 5 μm, as shown in Figure 3f.

3.4. Fabrication of ZnO-Nanowire Transistor Arrays. We fabricated wafer-scale arrays of ZnO-nanowire FETs using LSL. First, a 30-nm-thick Al_2O_3 dielectric layer was deposited on a 4-in. n^+-type Si wafer using atomic layer deposition. Then, an array of ZnO nanowires was fabricated on the substrate using selective immobilization via molecular patterns by LSL. Finally, source and drain electrodes using a bilayer evaporation of 10-nm-thick Ti followed by 50-nm-thick Au were deposited onto the ZnO nanowires using a

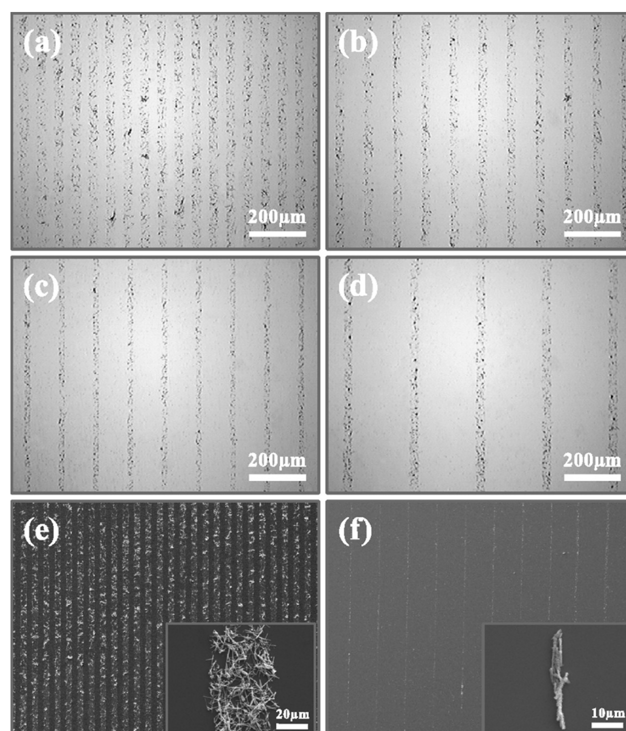


FIGURE 3. Optical microscopy and SEM images of the patterned ZnO nanowires of various feature sizes: (a) 30-μm lines and 30-μm spaces; (b) 30-μm lines and 70-μm spaces; (c) 20-μm lines and 90-μm spaces; (d) 30-μm lines and 200-μm spaces; (e) 40-μm lines and 40-μm spaces; (f) 5-μm lines and 70-μm spaces.

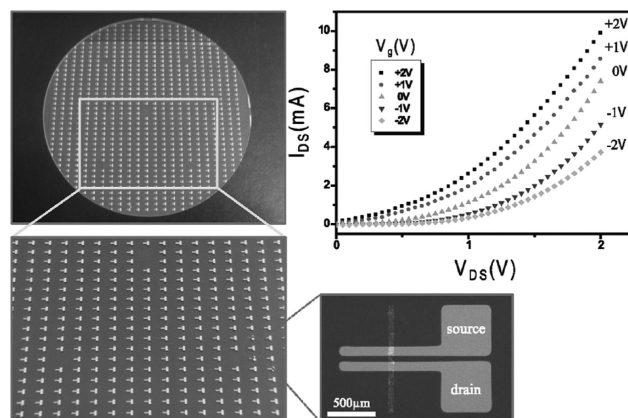


FIGURE 4. Optical microscopy and SEM images of ZnO-nanowire FETs and I_D−V_D curves of the back-gate ZnO-nanowire FET for V_G ranging from −2 to +2 V.

shadow mask. ZnO-nanowire FETs were thus obtained, with metal contacts functioning as source and drain electrodes and with the Si substrate as a back gate. Figure 4 shows optical microscopy and SEM images of such arrays of ZnO-nanowire FETs. Note that the channel length was 47 μm and the width was 50 μm. Figure 4 displays five drain current−drain voltage (I_D−V_D) output curves obtained under different gate voltages (V_G) varying from −2 to +2 V. The increase of the source−drain current with increasing gate voltage in output curves shows a general gating effect of n-type conductivity. The channel of the bottom-gate ZnO-nanowire FET is not fully depleted in the range of applied voltage from −2 to +2 V. This is probably due to the finite air gap between the ZnO nanowires and the gate oxide (41, 42). Also, the

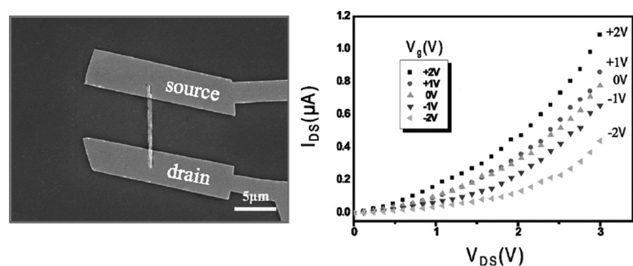


FIGURE 5. SEM image of a single ZnO-nanowire FET and I_D-V_D curves of the back-gate FET with a single ZnO nanowire for V_G ranging from −2 to +2 V.

output characteristics are not saturated, showing that the currents increase endlessly up to 2 V of the applied drain voltage. This is possibly attributed to exposure of the ZnO channel to air (43). For comparison, FETs were fabricated using a single ZnO nanowire. Figure 5 shows a SEM image of a single ZnO-nanowire FET and I_D-V_D output curves. All curves are analogous to those of the multi-ZnO-nanowire FETs shown in Figure 4, which means that there is no significant contact resistance among the nanowires in the multi-ZnO-nanowire FETs. The possible reason for this low contact resistance may be the formation of solid bridges among the ZnO nanowires (44, 45).

4. CONCLUSIONS

We developed a new large-area fabrication method of patterned ZnO-nanowire arrays using surface-pattern-directed assembly. In the present method, surface molecular patterns were prepared by LSL, which can be adopted in automated printing machines that generate patterned ZnO-nanowire arrays on large-area substrates. As a proof of concept, we performed wafer-scale fabrication of ZnO-nanowire transistors with high yield and uniformity.

Acknowledgment. This work was supported by the Korea Science and Engineering Foundation (KOSEF) grant funded by the Korea government (MEST) (Grant 20090092807) and by Seoul R&BD Program (Grant ST090839) and by the "SystemIC2010" project of Korea Ministry of Commerce, Industry and Energy and by a Nano R&D program through the National Research Foundation of Korea funded by the Ministry of Education, Science and Technology (Grant 2009-0083208) and by a grant (Grant F0004031-2009-32) from the Information Display R&D Center, one of the 21st Century Frontier R&D Program funded by the Ministry of Knowledge Economy of Korean government. This work also supported by the Research fund of HYU (HYU-2009-T).

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AM900580V